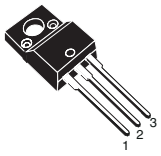
# STP12NK60Z
# STF12NK60Z

## N-channel 650 V @Tjmax- 0.53 Ω - 10 A - TO-220 /TO-220FP Zener-protected SuperMESH™ Power MOSFET

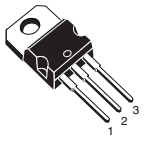
## Features

| Type | $V_{DSS}$ (@Tjmax) | $R_{DS(on)}$ max | $I_D$ | $P_W$ |
|---|---|---|---|---|
| STP12NK60Z | 650 V | <0.640 Ω | 10 A | 150 W |
| STF12NK60Z | 650 V | <0.640 Ω | 10 A | 35 W |

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



TO-220FP



TO-220

## Application

- Switching applications

## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, specialties is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage Power MOSFETs.

**Figure 1. Internal schematic diagram**

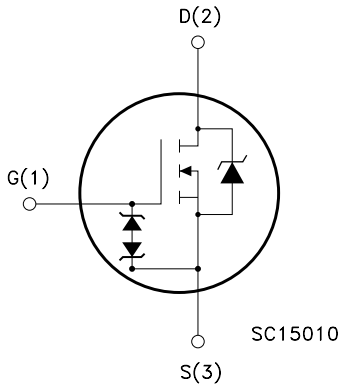



**Table 1. Device summary**

| Order codes | Marking | Package | Packaging |
|---|---|---|---|
| STP12NK60Z | P12NK60Z | TO-220 | Tube |
| STF12NK60Z | F12NK60Z | TO-220FP | Tube |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | TO-220 | TO-220FP | |
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 600 | | V |
| $V_{GS}$ | Gate-source voltage | ±30 | | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 10 | 10 (1) | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 6.3 | 6.3 (1) | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 40 | 40 (1) | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 150 | 35 | W |
| | Derating factor | 1.2 | 0.27 | W/°C |
| $V_{ESD(G-S)}$ | Gate source ESD (HBM-C=100 pF, R=1.5 kΩ) | -- | 2500 | V |
| dv/dt (3) | Peak diode recovery voltage slope | 4.5 | | V/ns |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t =1 s;$T_C$ = 25 °C) | -- | 2500 | V |
| $T_{stg}$ | Storage temperature | -55 to 150 | | °C |
| $T_j$ | Max operating junction temperature | 150 | | °C |

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD}$ ≤10 A, di/dt ≤ 200 A/µs, $V_{DD}$ = 480 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | TO-220 | TO-220FP | |
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.83 | 3.6 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 62.5 | | °C/W |
| $T_l$ | Maximum lead temperature for soldering purpose | 300 | | °C |

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AS}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max) | 10 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting Tj=25°C, $I_D$=$I_{AS}$, $V_{DD}$=50 V) | 260 | mJ |

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 5. On/off**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating<br>$V_{DS}$ = Max rating, $T_C$=125 °C | | | 1<br>50 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10 V, $I_D$ = 5 A | | 0.53 | 0.64 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$=10 V, $I_D$ = 5 A | | 9 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V, f = 1 MHz,<br>$V_{GS}$ = 0 | | 1740<br>195<br>49 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (2) | Equivalent output capacitance | $V_{GS}$ = 0, $V_{DS}$ = 0 to 480 V | | 101 | | pF |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$ = 300 V, $I_D$ = 5 A,<br>$R_G$=4.7 Ω<br>$V_{GS}$ = 10 V<br>*(see Figure 17)* | | 22.5<br>18.5<br>55<br>31.5 | | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$ = 480 V, $I_D$ = 10 A,<br>$V_{GS}$ = 10 V<br>*(see Figure 18)* | | 59<br>10<br>32 | | nC<br>nC<br>nC |

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DS}$

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (1) | Source-drain current<br>Source-drain current (pulsed) | | | | 10<br>40 | A<br>A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 10 A, $V_{GS}$ = 0 | | | 1.6 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 10 A, di/dt = 100 A/µs<br>$V_{DD}$ = 50 V<br>*(see Figure 22)* | | 358<br>3<br>17 | | ns<br>µC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 10 A, di/dt = 100 A/µs<br>$V_{DD}$ = 50 V, $T_j$ = 150 °C<br>*(see Figure 22)* | | 460<br>4.2<br>18.2 | | ns<br>µC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

**Table 8. Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $BV_{GSO}$ (1) | Gate-Source breakdown voltage | Igs=± 1 mA (open drain) | 30 | | | V |

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area for TO-220**

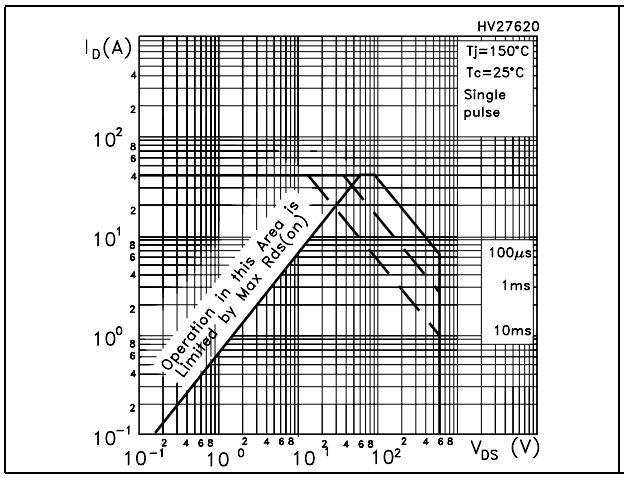



**Figure 3. Thermal impedance for TO-220**

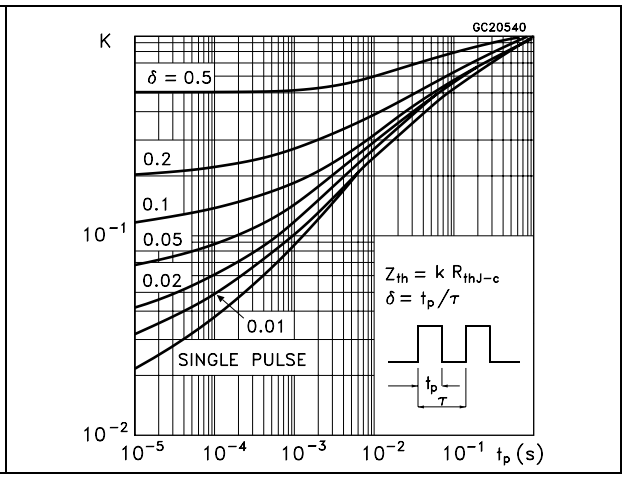



**Figure 4. Safe operating area for TO-220FP**

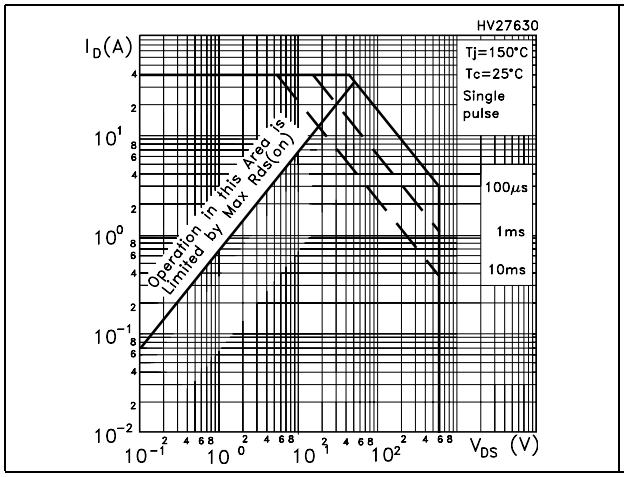



**Figure 5. Thermal impedance for TO-220FP**

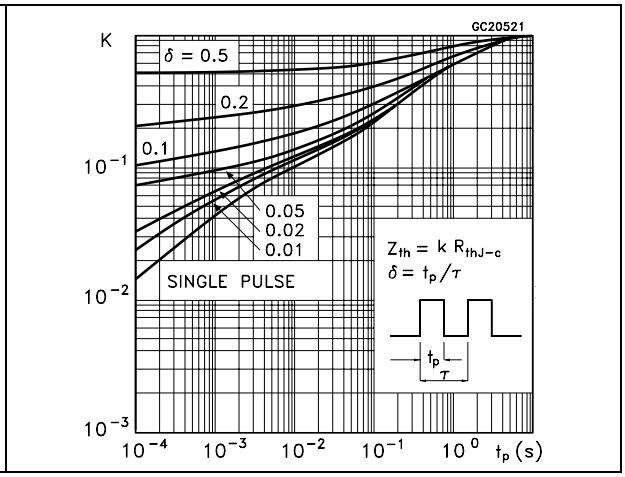



**Figure 6. Output characteristics**

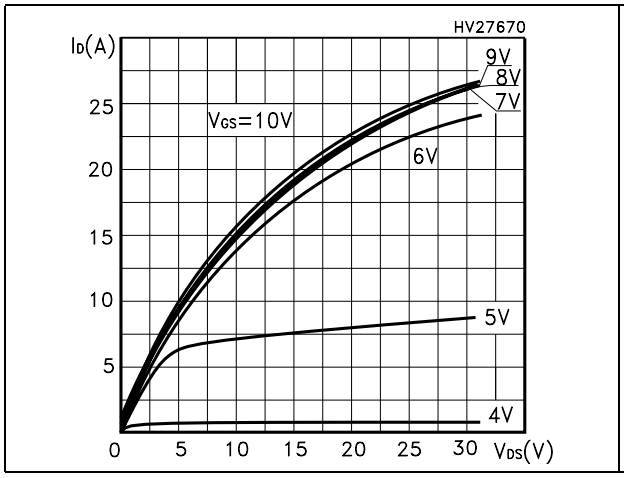



**Figure 7. Transfer characteristics**

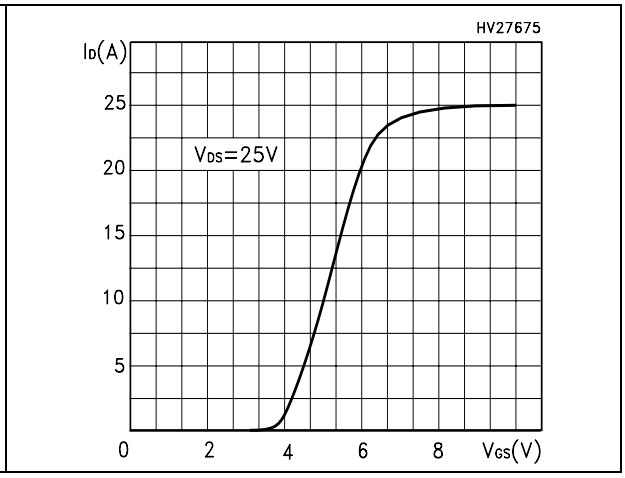


**Figure 8. Transconductance**

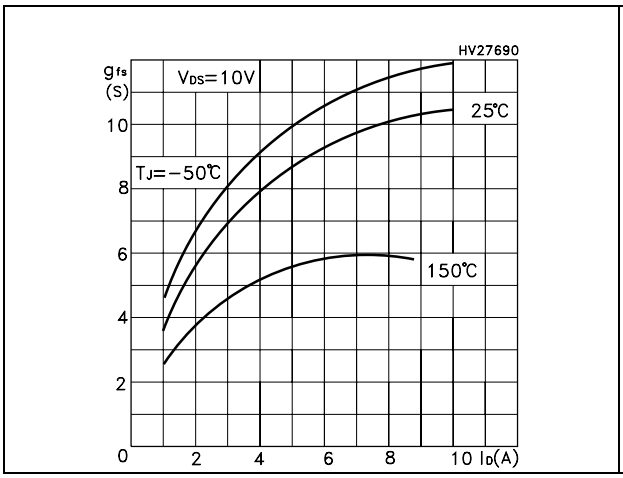



**Figure 9. Static drain-source on resistance**

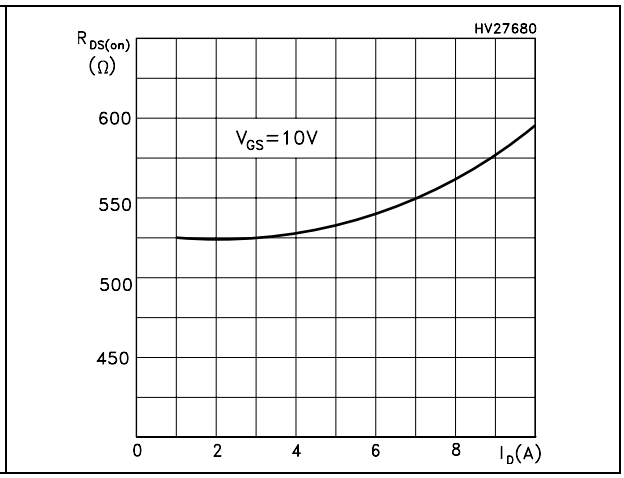



**Figure 10. Gate charge vs gate-source voltage**

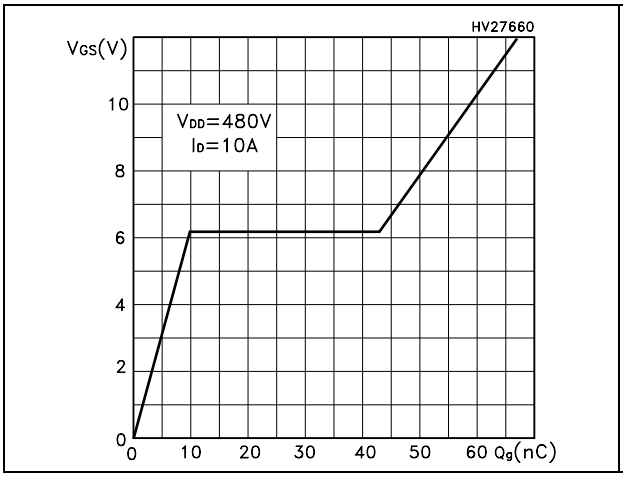



**Figure 11. Capacitance variations**

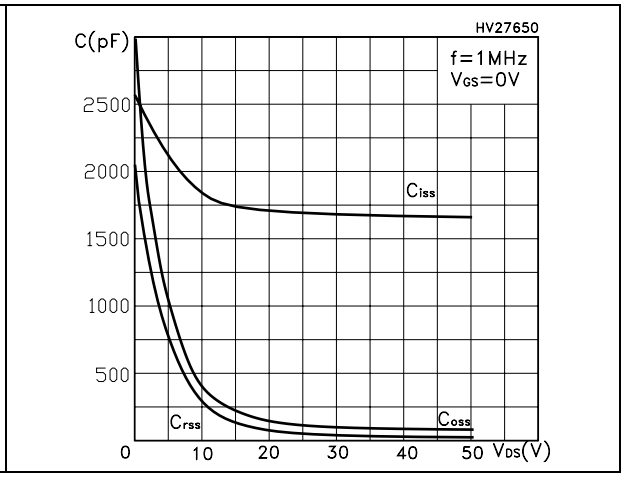



**Figure 12. Normalized gate threshold voltage vs temperature**

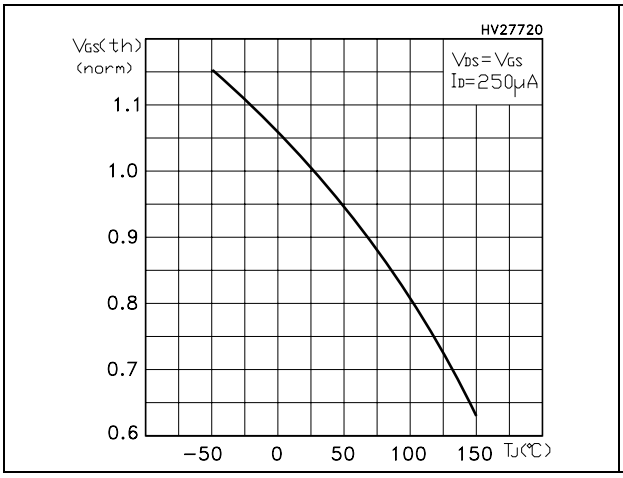



**Figure 13. Normalized on resistance vs temperature**

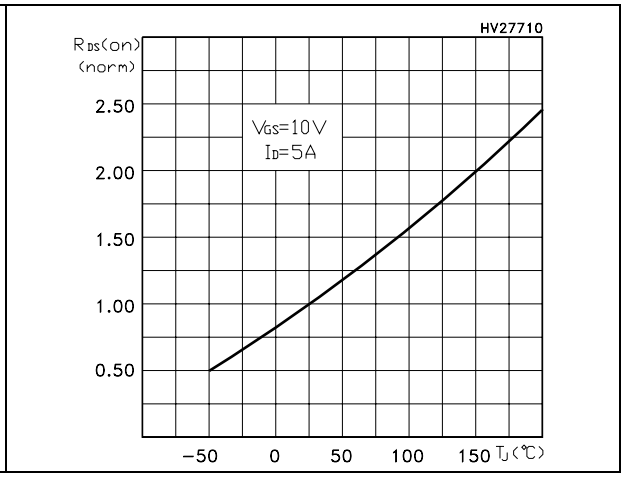


**Figure 14. Source-drain diode forward characteristics**

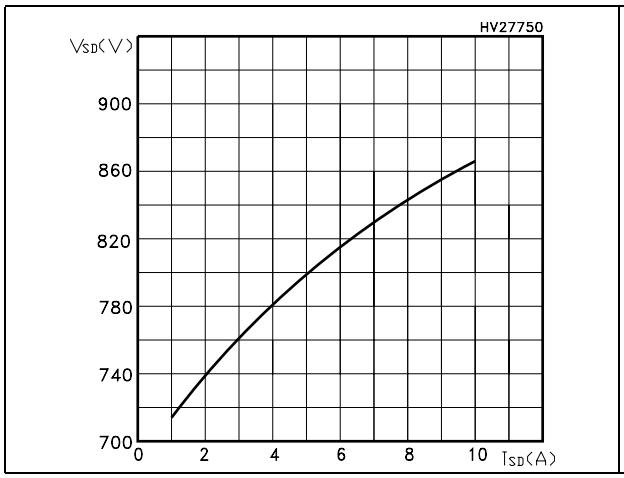



**Figure 15. Normalized breakdown voltage vs temperature**

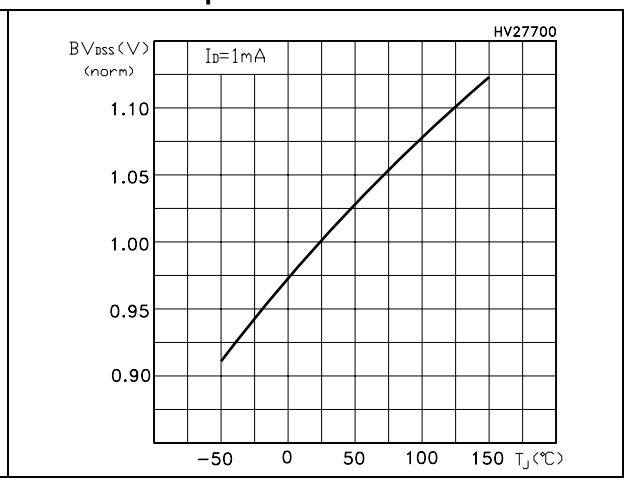
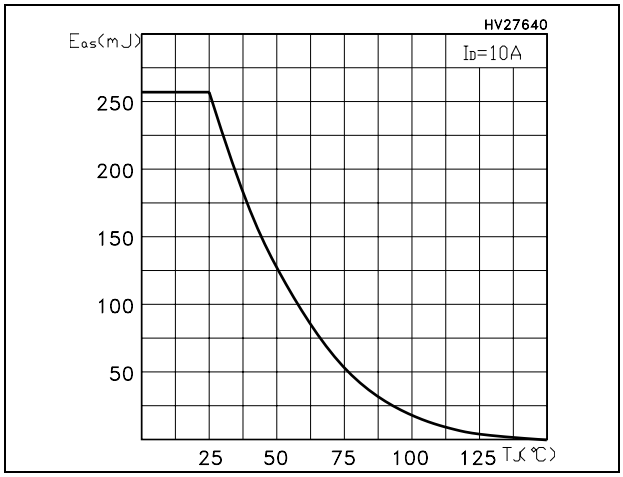



**Figure 16. Maximum avalanche energy vs temperature**



# 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**

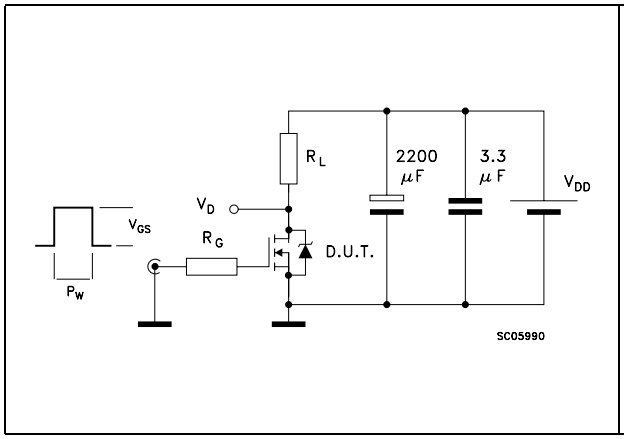



**Figure 18. Gate charge test circuit**

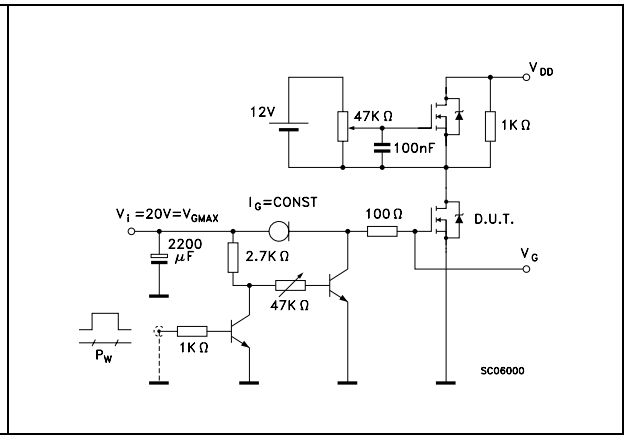



**Figure 19. Test circuit for inductive load switching and diode recovery times**

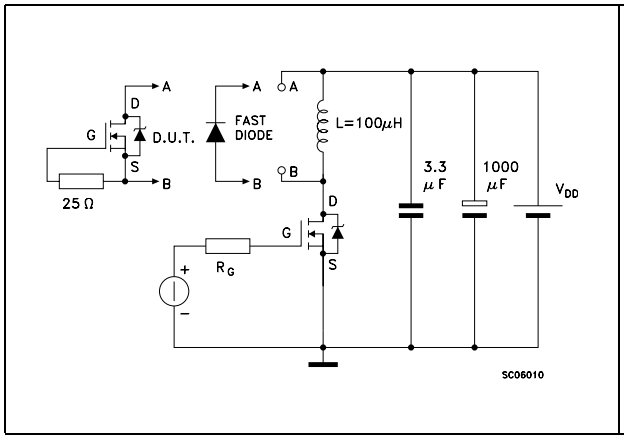



**Figure 20. Unclamped inductive load test circuit**

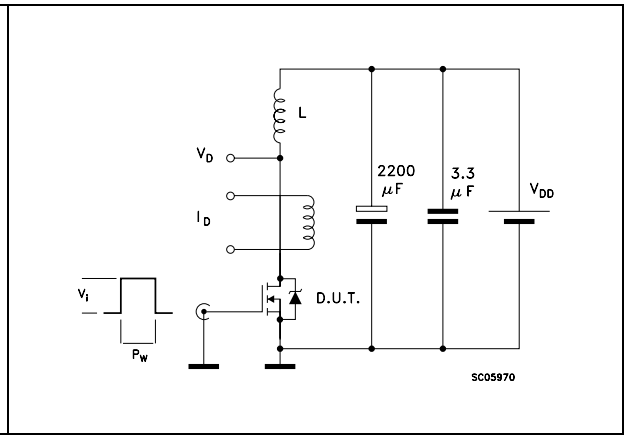



**Figure 21. Unclamped inductive waveform**

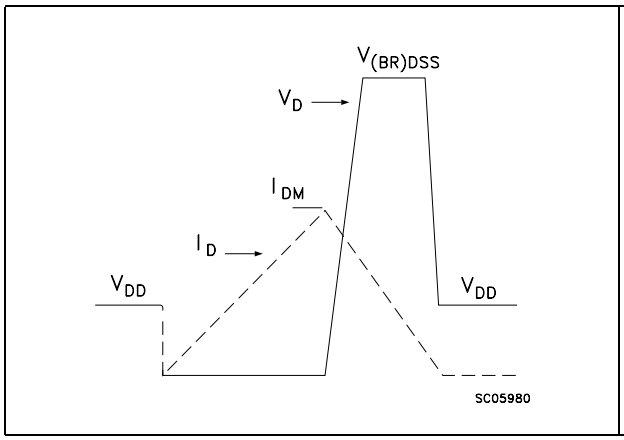
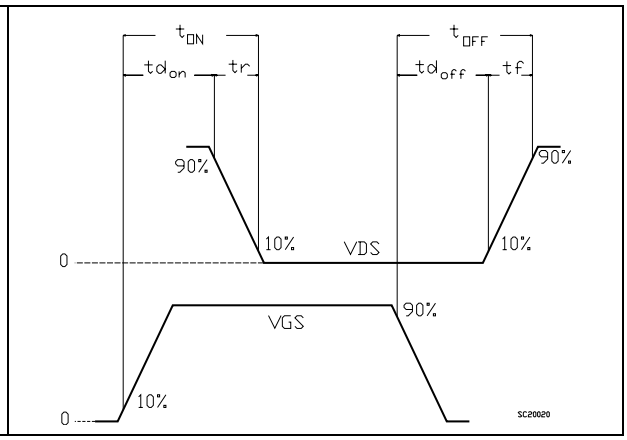



**Figure 22. Switching time waveform**

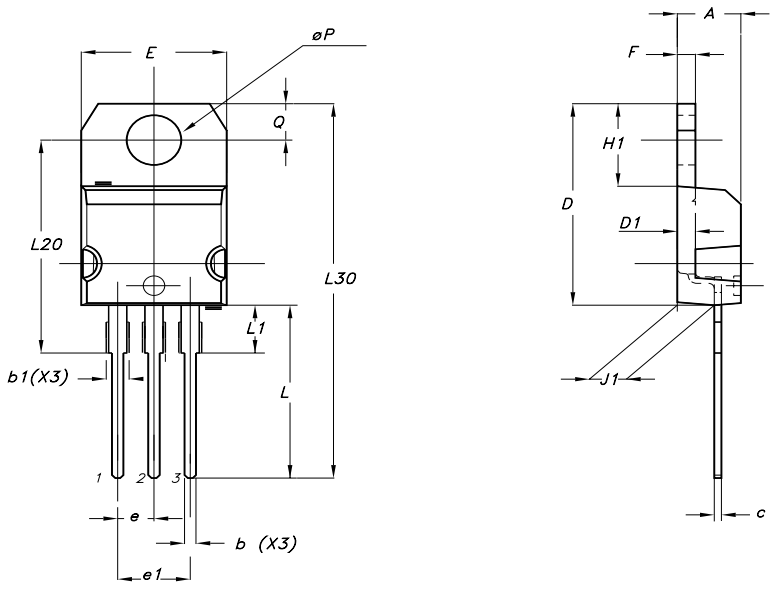


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

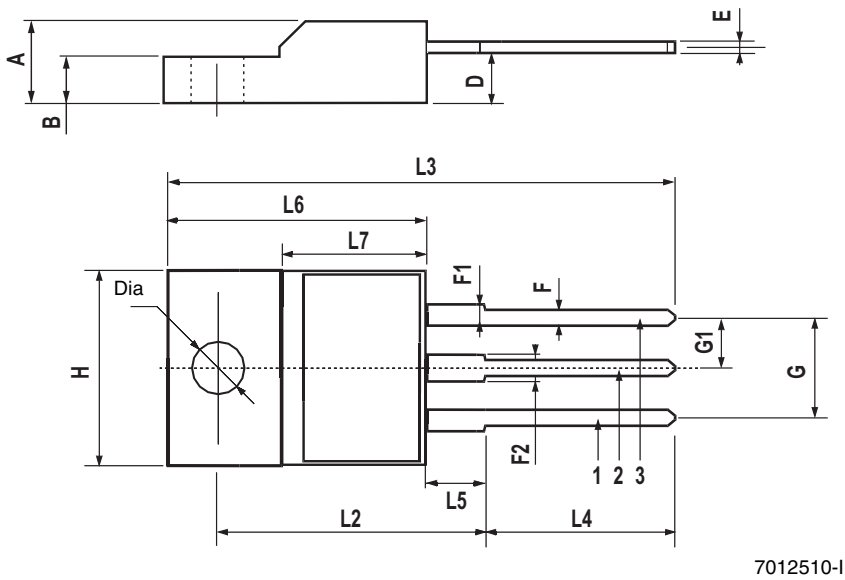
## TO-220 mechanical data

| Dim | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 4.40 | | 4.60 | 0.173 | | 0.181 |
| b | 0.61 | | 0.88 | 0.024 | | 0.034 |
| b1 | 1.14 | | 1.70 | 0.044 | | 0.066 |
| c | 0.49 | | 0.70 | 0.019 | | 0.027 |
| D | 15.25 | | 15.75 | 0.6 | | 0.62 |
| D1 | | 1.27 | | | 0.050 | |
| E | 10 | | 10.40 | 0.393 | | 0.409 |
| e | 2.40 | | 2.70 | 0.094 | | 0.106 |
| e1 | 4.95 | | 5.15 | 0.194 | | 0.202 |
| F | 1.23 | | 1.32 | 0.048 | | 0.051 |
| H1 | 6.20 | | 6.60 | 0.244 | | 0.256 |
| J1 | 2.40 | | 2.72 | 0.094 | | 0.107 |
| L | 13 | | 14 | 0.511 | | 0.551 |
| L1 | 3.50 | | 3.93 | 0.137 | | 0.154 |
| L20 | | 16.40 | | | 0.645 | |
| L30 | | 28.90 | | | 1.137 | |
| ∅P | 3.75 | | 3.85 | 0.147 | | 0.151 |
| Q | 2.65 | | 2.95 | 0.104 | | 0.116 |



## TO-220FP mechanical data

| Dim. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | Min. | Typ | Max. | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 | 0.173 | | 0.181 |
| B | 2.5 | | 2.7 | 0.098 | | 0.106 |
| D | 2.5 | | 2.75 | 0.098 | | 0.108 |
| E | 0.45 | | 0.70 | 0.017 | | 0.027 |
| F | 0.75 | | 1.00 | 0.030 | | 0.039 |
| F1 | 1.15 | | 1.50 | 0.045 | | 0.067 |
| F2 | 1.15 | | 1.50 | 0.045 | | 0.067 |
| G | 4.95 | | 5.20 | 0.195 | | 0.204 |
| G1 | 2.40 | | 2.70 | 0.094 | | 0.106 |
| H | 10 | | 10.40 | 0.393 | | 0.409 |
| L2 | | 16 | | | 0.630 | |
| L3 | 28.6 | | 30.6 | 1.126 | | 1.204 |
| L4 | 9.80 | | 10.60 | 0.385 | | 0.417 |
| L5 | 2.9 | | 3.6 | 0.114 | | 0.141 |
| L6 | 15.90 | | 16.40 | 0.626 | | 0.645 |
| L7 | 9 | | 9.30 | 0.354 | | 0.366 |
| Dia | 3 | | 3.2 | 0.118 | | 0.126 |



# 5 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 12-Apr-2004 | 1 | First release |
| 06-Sep-2005 | 2 | Inserted ecopack indication |
| 13-Sep-2005 | 3 | Final version |
| 05-Sep-2006 | 4 | The document has been reformatted |
| 26-Apr-2007 | 5 | The document has been updated on *1: Electrical ratings* |
| 25-Jan-2008 | 6 | Modified: dv/dt value on *Table 2: Absolute maximum ratings* |